

**Department of Physics**

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| Course Number | COE 328 |
| Course Title | Digital Circuits |
| Semester/Year | Fall 2021 |
| Instructor | Dr. Reza Sedaghat |
| TA Name | Sajjad Rostami Sani |

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| Lab/Tutorial Report No. | 5 |
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| Report Title | Lab 5 |

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| Section No. | 03 |
| Submission Date | 20-11-2021 |
| Due Date | 29-11-2021 |

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| Student Name | Student ID | Signature\* |
| Ahmad El-Gohary | 501011852 |  |

\*By signing above, you attest that you have contributed to this submission and confirm that all work you have contributed to this submission is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a “0” on the work, an “F” in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at:

http://www.ryerson.ca/content/dam/senate/policies/pol60.pdf

**Objective**

The objective of this lab was to simulate the operation of a sequential circuit and to design a finite state machine that cycles through the digits of my student number using the assigned state diagram.

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**Procedure**

* To get the assigned state machine take the last 4 digits of my student number and divide it by the number of states to get the remainder.
* The remainder is the state number

1852/13 has a remainder of 6

Assigned Finite State Machine:

Diagram

Description automatically generated

The machine shows that when data in is equal to 0 the state is assigned to itself but when data in is equal to 1 it is assigned to the state to its right for example: when data in for s0 is 1 s0 is assigned to s4.

Value of s0 to s8 is assigned the value its respective student number digits according to the FSM.

Table

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Implementing the previous information into VHDL code provided in the lab manual page 6:Text

Description automatically generatedGraphical user interface, text, application

Description automatically generated with medium confidenceGraphical user interface

Description automatically generated with low confidenceText

Description automatically generated with medium confidence

Converting the previous VHDL code into a block diagram:

Text

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7 segment display code from lab 3:*Table

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Converting the previous VHDL code into a block diagram:

Table

Description automatically generated

Connecting the 7-segment display with the FSM in a circuit:

Diagram

Description automatically generated

Waveform for the sequential circuit:

A picture containing timeline

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**References**

Brown, S. D., & Vranesic, Z. G. (2009). *Fundamentals of Digital Logic with VHDL Design*. New York, United States: McGraw-Hill Education.